#13/B
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Harrison

PATENT
740756-2101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of:	)	Art Unit:	2813
Shunpei YAMAZAKI et al.	)	Examiner:	E. Pert
Application No.: 09/502,675	)		
Filed: February 11, 2000	)		
For: SEMICONDUCTOR DEVICE METHOD OF MANUFACTURING THEREFOR	)		

AMENDMENT

Honorable Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

In response to the Examiner's non-final Office Action mailed September 13, 2001, the period for responding having been extended one (1) month, please consider the following amendments and remarks in connection with the above-identified application.

IN THE SPECIFICATION:

Please amend the specification as follows:

At Page 40, paragraph 3 spanning to Page 41, paragraph 2, replace with the following:

B1

--Fig. 14C shows an example of the structure of a sampling circuit TFT. The n-channel TFT of this circuit is a single gate, and second impurity regions that become LDD regions are formed on both the source side and the drain side. The length of the LDD regions 205 and 206 which do not overlap the gate electrode may be formed in the range of 0.5 to 3.0 μm, and both are preferably made of equal length. The objective of lowering the off current value, and the objective of preventing degradation of the TFT due to the hot carrier effect, can both be achieved at the same time by these LDD regions.

Fig. 14D is a structure suitable to a driver circuit operated at a high speed by a driver voltage of approximately 1.5 to 5 V. Third impurity regions that overlap the gate electrode are